

System Technical Document D1f

Command Protocol Goals

- Easy to adapt to different systems
- Works in a tree structure
- Clear Grouping of commands
 - Easy to remember
- Easy Debugging
 - commands, addresses have different values
- Compounded commands

Values for Commands (hex)

- A0-A4: **A**udio commands
- A8-AF: Table unit commands
- B0-B8: **G**roup
- C0-CC: **C**ontrol, **C**onfiguration
- CE : **C**ommand **E**nd, Synchronization
- D0-DA: **V**ideo Commands
- E1-E6: **E**rror Codes

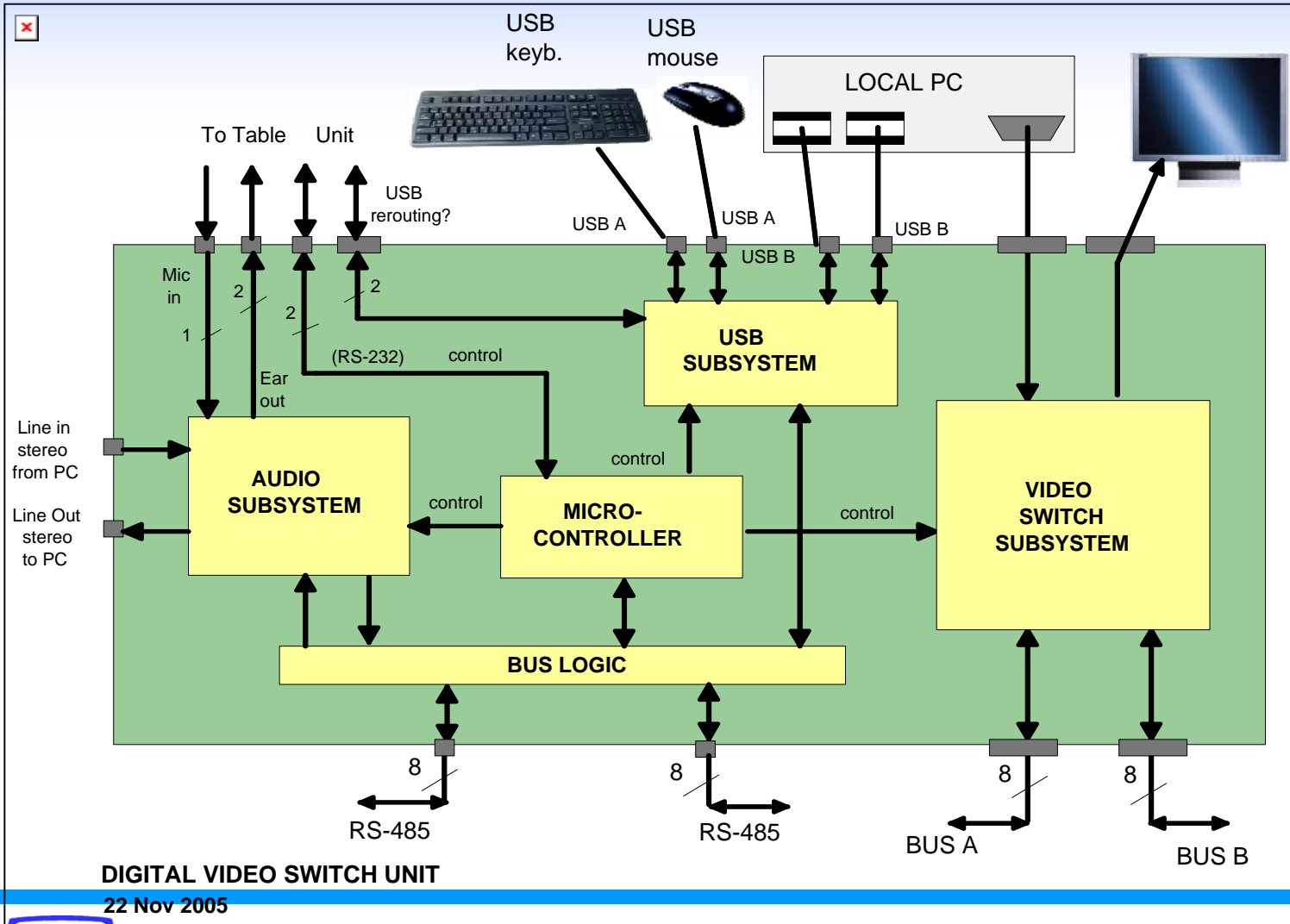
Command Examples

- Screen Transfer to all others
 - <D1h> <source> <CEh>
- Audio Connection between two PCs
 - <A4h> <source1> <source2> <CEh>
- Set Group 4
 - <B4h> <Addr1> <Addr2>... <CEh>

Values for Commands and Addresses

Meaning of byte	Address	Hex address	Address in configuration
PC address of teacher	0	0	0
PC addresses	1-127	1-7Fh	1-127
(Address for all)	(128)	(80h)	Not in use
Hub addresses	129-159	81h-9Fh	Hub 1-31
Commands	160-223	A0h-C9h	
Command End from Master	206	CEh	
Command End from Slave	207	CFh	
Video Commands	208-224	D0-DAh	
Error codes	225-239	E1h – EFh	
Null Address	240	F0h	240
Groups 1,2,3,4	241-244	F1-F4h	

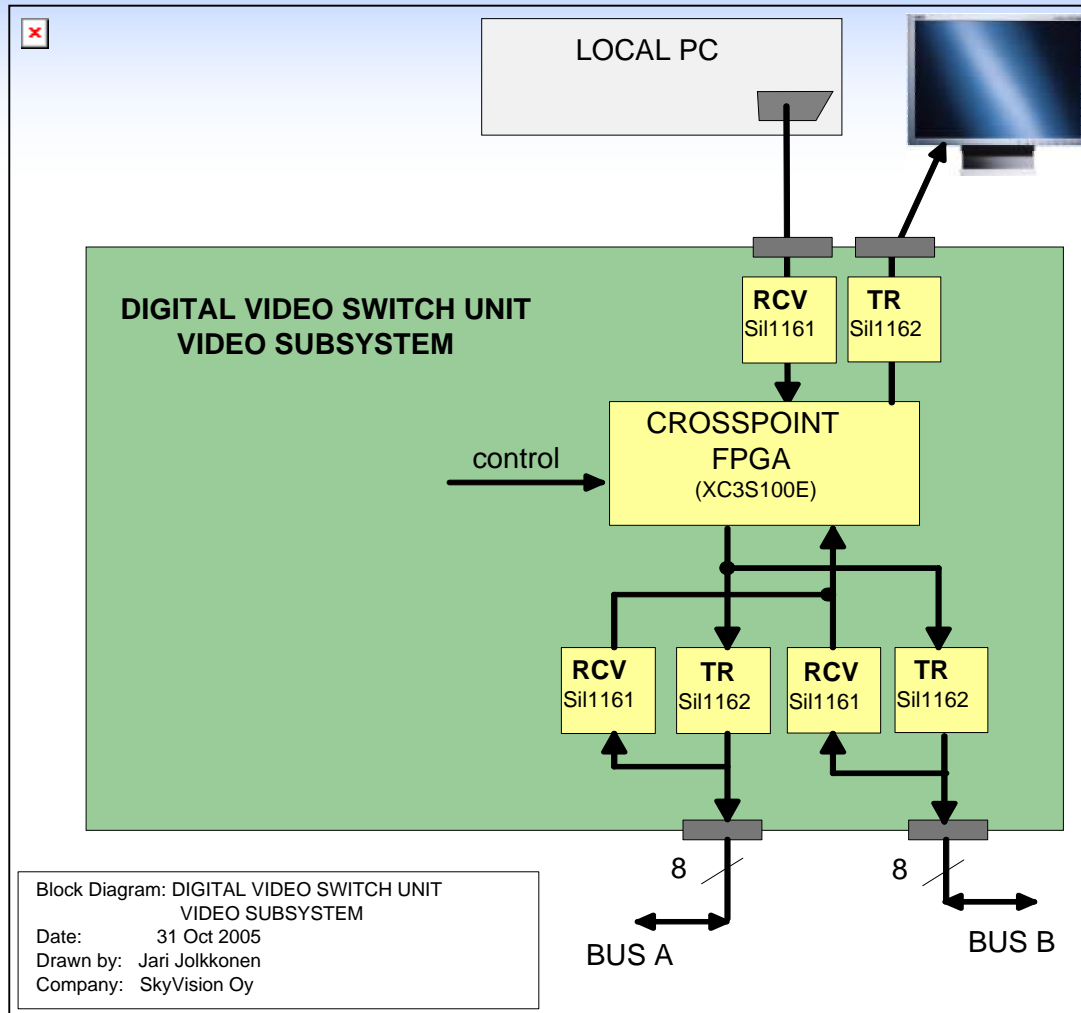
Digital Video Switch Unit



DIGITAL VIDEO SWITCH UNIT
22 Nov 2005



Video Switch Subunit



Supported Display modes

Resolution name	Resolution	Dot frequency (pixel clock) MHz	Refresh rate (Hz)	Horizontal frequency (kHz)	Notes
4:3 modes					
SVGA	800 x 600	36 – 56	56 – 85	35 – 53	
XGA	1024 x 768	45 – 94	60 – 85	35 – 69	
SXGA	1280 x 1024	108 – 157	60 – 85	64 – 91	
	1400 x 1050	101 - 180	60 - 85	65 - 85	*1)
UXGA	1600 x 1200	162 - 229	60 - 85	75 – 106	
Wide modes					
(720p)	1280 x 768	68 - 117	60 - 85	47 – 69	*1)
	1680 x 1050	119 – 214	60 - 85	65 - 94	*1)
HDTV	1920 x 1200	154 - 281	60 - 85	74 - 107	*1)
HDTVplus	1920 x 1440	234, 297	60, 75	90, 112	*1)

DVI Transmitters and Receivers

DVI Transmitter	Manufacturer	Price (USD)	Footprint	Frequency MHz	Remarks
Sil 1162	Silicon Image	2.53	TSSOP 48	25 - 165	
Sil 1172	Silicon Image	6.53	TSSOP 48	25 - 225	
Sil 1160	Silicon Image	3.19	TQFP 100	25 - 165	
TFP410	TI	3.00	TQFP 64	25 - 165	
VT 1632	Via Techn.		TQFP 64	25 - 165	distribution ?
CH7307C	Chrontel		TQFP 48	25 - 165	distribution? preli datasheets
DVI Receiver					Equalization
Sil 1161	Silicon Image	4.93	TQFP 100	25 - 165	Yes
Sil 1171	Silicon Image	10.67	TQFP 100	25 - 225	Yes
TFP401A	TI	4.00	TQFP 100	25 - 165	No
Cable Equalizers					
MAX3815	Maxim	5.00	TQFP 48	25 - 165	Yes

FPGA in Digital Video Switch and HUB

Double Data Rate

- DDR is the trickiest part in FPGA design
- with 165 MHz, you need appr. 1.515 ns setup and hold time windows
- 50% duty-cycle
- SiI DVI chips do not de-skew clock, hence cascading DVI R + FPGA + DVI T requires de-skew in FPGA
- key elements with FPGA:
 - PLL/DLL
 - DDR support
 - efficient clocking scheme
 - asynchronous FIFO
 - must be capable of de-skewing 2 x internal clock and 3 x external clock
 - system speed 250 MHz +

FPGA vendor evaluation

- Altera
 - second to Xilinx technologywise
 - at the moment, more expensive than Xilinx
 - synthesis tool costs 493\$ plus ModelSim
 - price 11,6\$
- Lattice
 - at the moment the most inexpensive chips with small volumes
 - their PLL is quite new technology, not mature yet?
 - synthesis and simulator cost another 350\$
 - neither SkyVision or VTT have prior experience
 - price 6,55\$
- Xilinx
 - has long been the technological leader
 - can fulfil all the SCREENS specs.
 - free Synthesis and CoreGen since WebPack v8. ModelSim will cost
 - SkyVision has employed Xilinx since 1998 and has a very thorough expertise on Xilinx tools and architecture at video electronics
 - price 8,4\$

Why Xilinx?

- fastest time-to-market
- Xilinx capabilities have been quite thoroughly tested against system specs.
- chip price is still negotiable. At the moment this could be 7 – 7,5\$ but as the production starts, it will be even less

μ Controller selection for Digital Video Switch and HUB

Requirements for μ Controller

1. speed
2. 2 x UART
3. optimized for C code
4. on-chip memory (Flash, RAM, EEPROM)
5. IO capabilities
6. large selection of different chip alternatives
7. availability of low-cost and effective C compiler
8. price

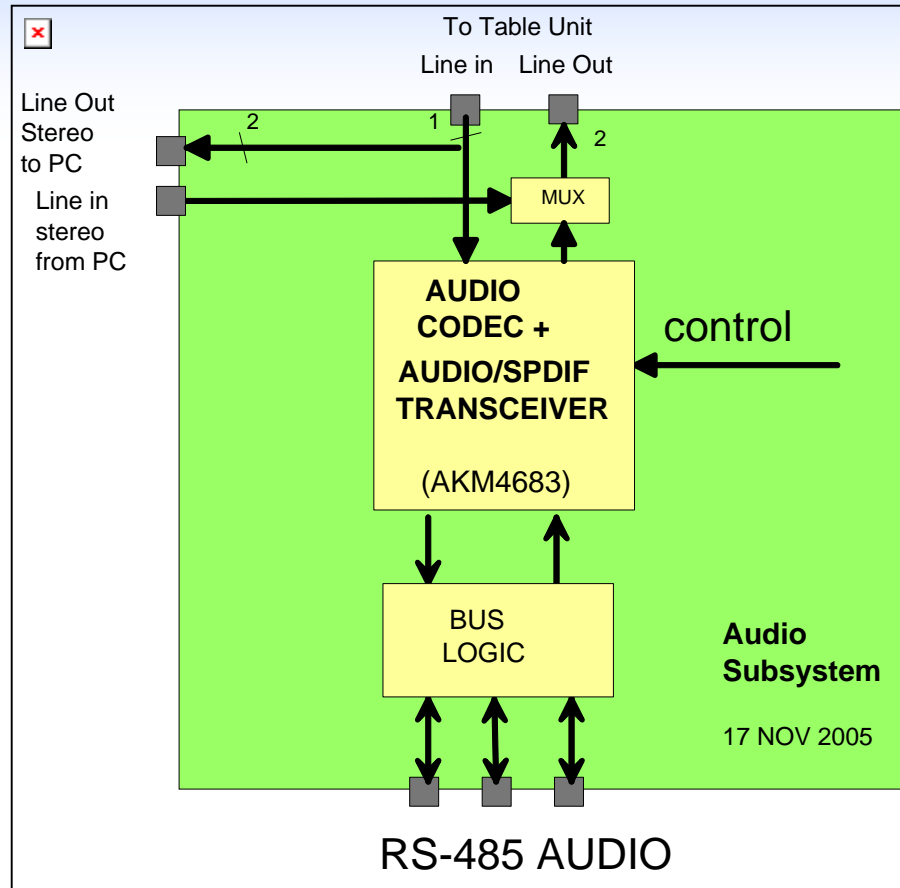
AVR

- Atmel AVR is a very good choice
- SkyVision has employed Intel-51 since 1994 but no longer sees it viable in new designs
- 4 C compilers were evaluated. CodeVision turned out the best choice costing 225€

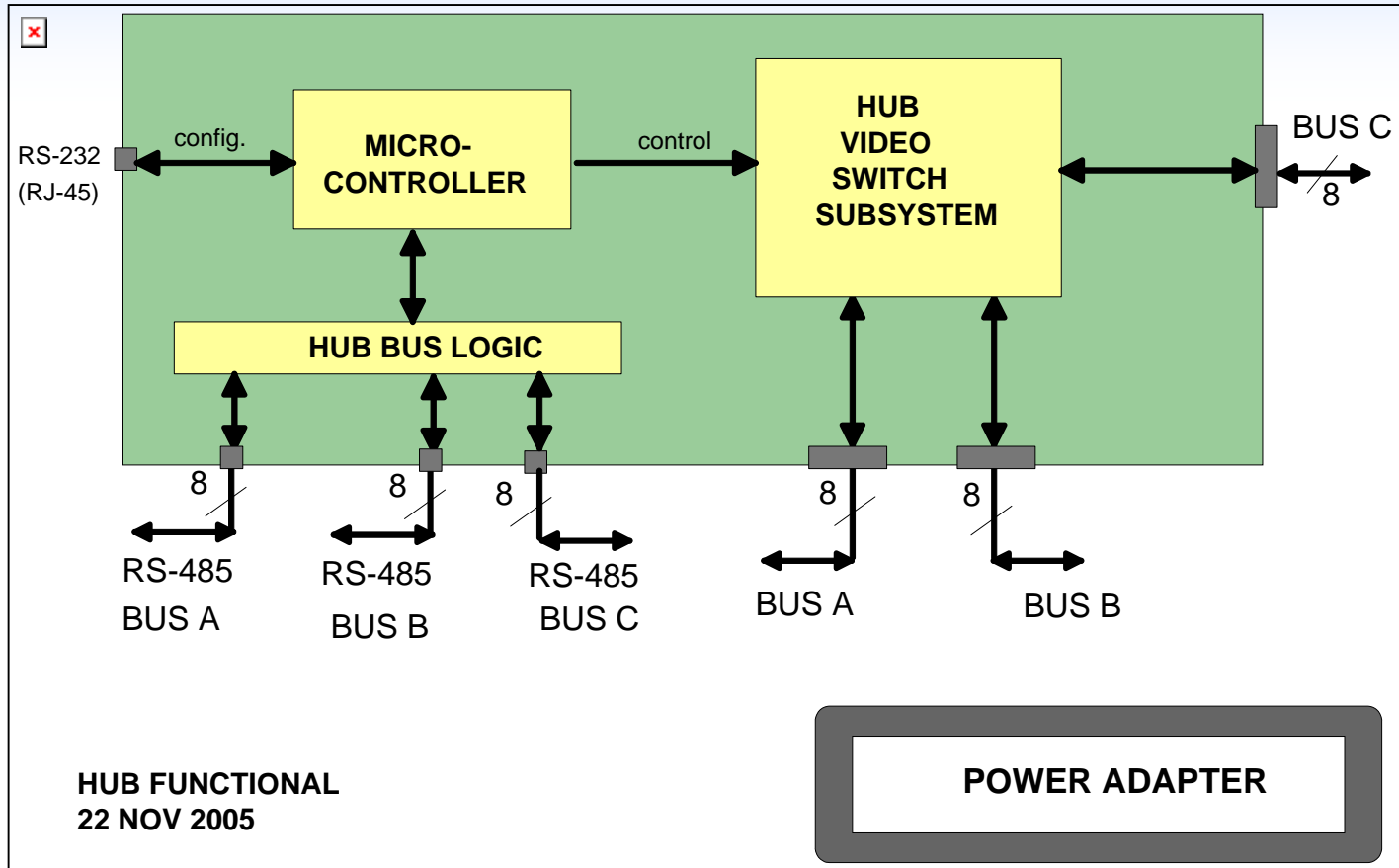
Selected AVR

- ATmega162-16AI
 - 16 kB Flash
 - 512 B EEPROM
 - 1 kB RAM
 - 35 IO pins
 - 2 x UART
 - 2 x 16-bit timers
 - 2.7V – 5.5V voltage range
 - TQFP32
 - **2,77€** per unit (VAT 0%, at 160 pcs quantities)

Audio Subunit



HUB



HUB Video Subsystem

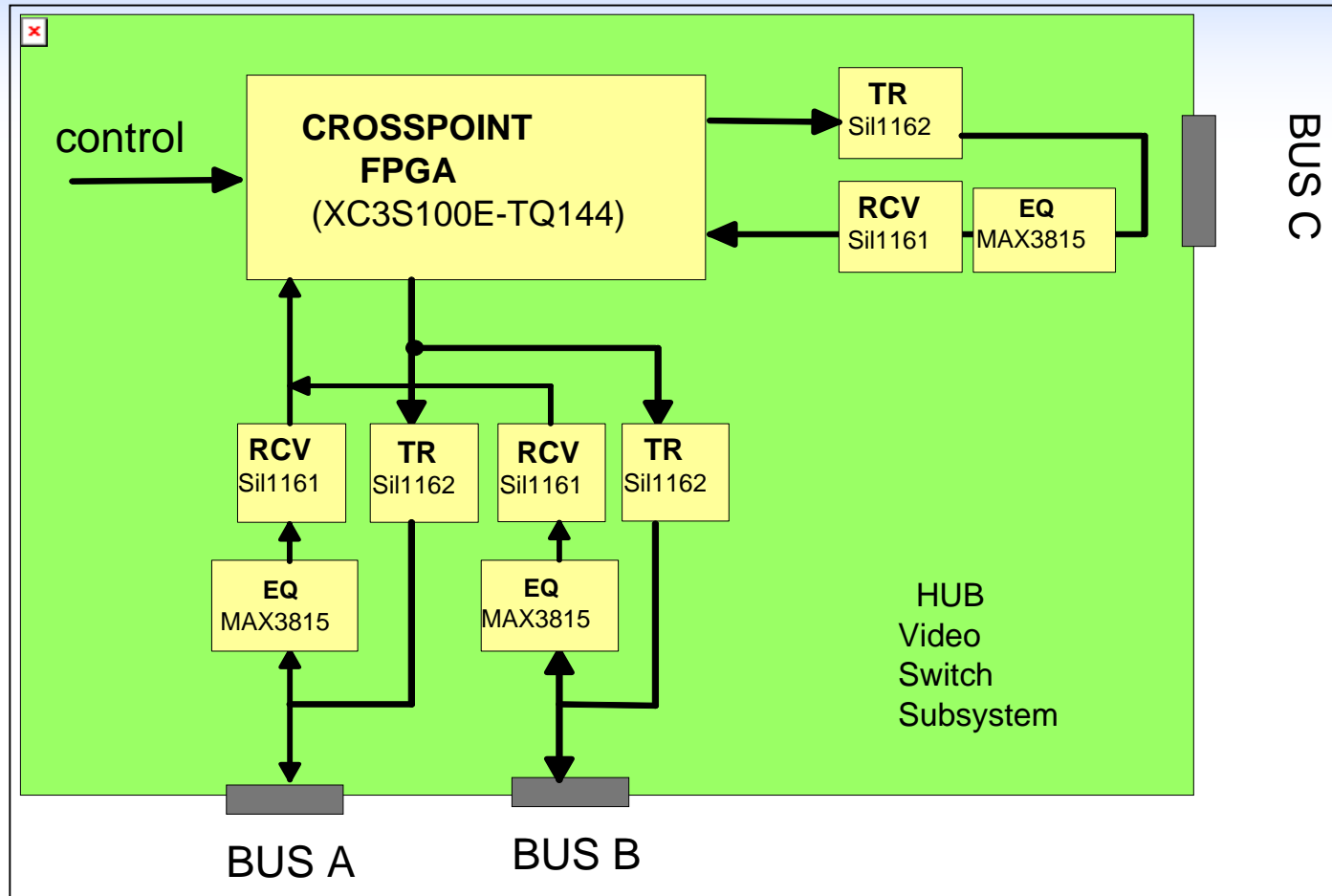


Table Unit Block Diagram

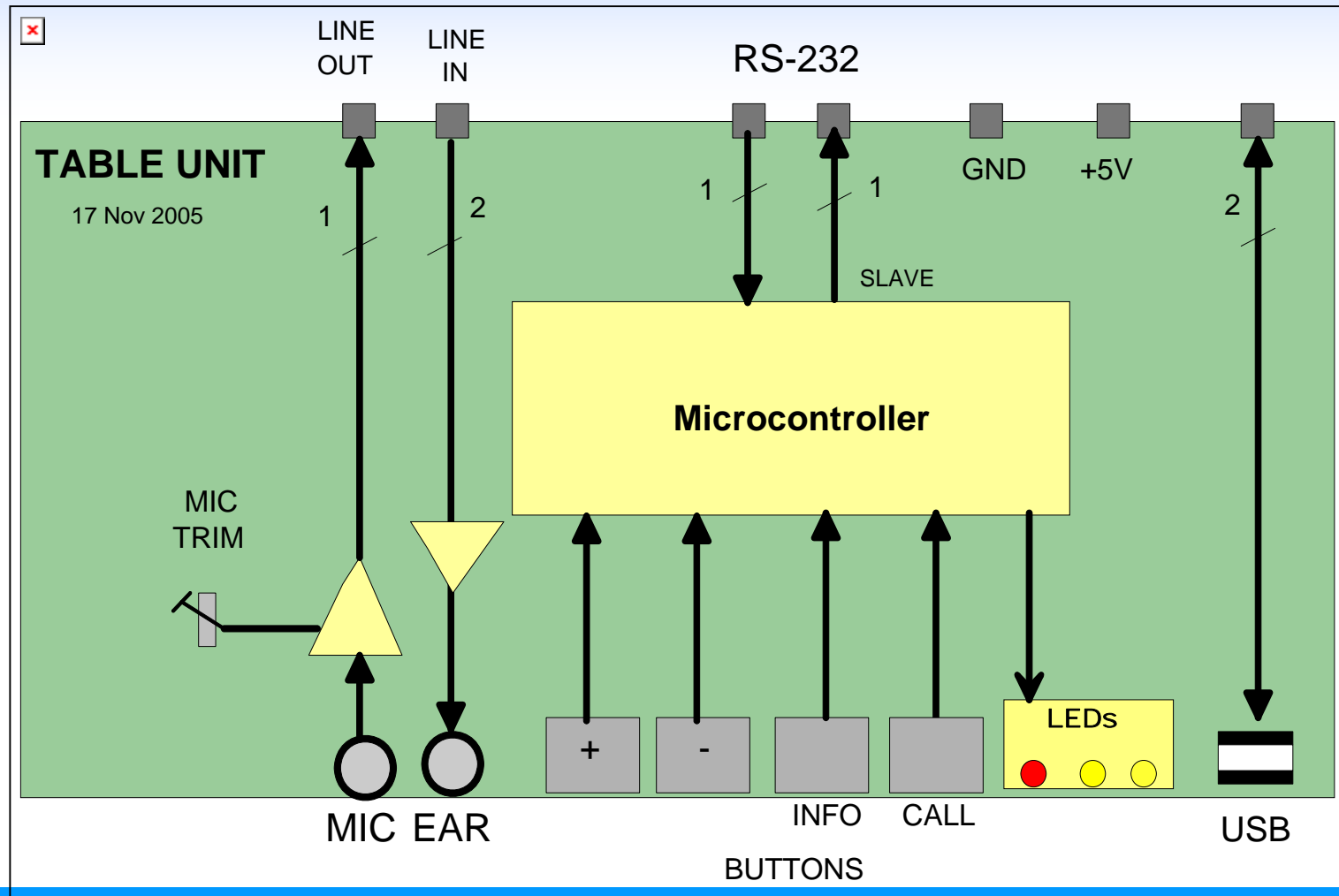


Table Unit Commands proposal

- Simple Protocol
- Same Command values than on the Bus